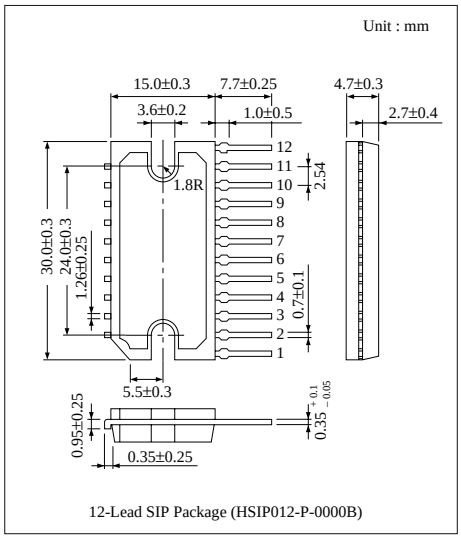
AN7158N

Dual 7.5W Audio Power Amplifier Circuit

■ Overview

The AN7158N is an integrated circuit designed for power amplifier of 7.5W (16V, 4Ω) output with low noise and low distortion, and it suits TV set with multi-sound. Stereo operation is enabled due to incorporating two amplifiers on one chip. 12-pin SIL package enabled compact and high-densely mounted set.

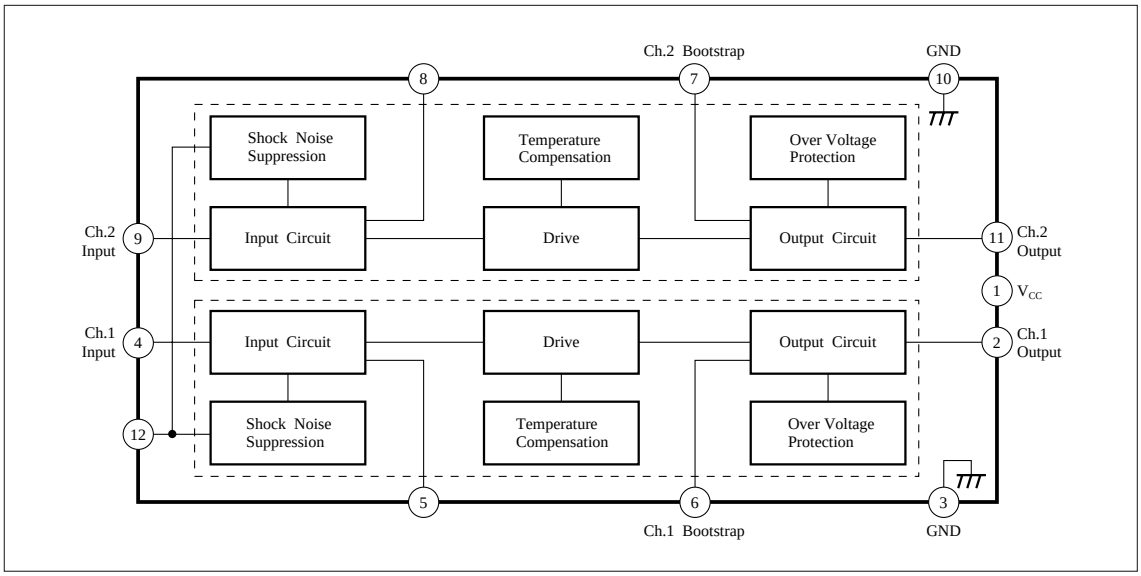


12-Lead SIP Package (HSIP012-P-0000B)

■ Features

- Incorporating protection circuits (surge, thermal protection and etc.)
- Automatic operating point stabilizer circuit
- Low distortion, low 1/f noise
- Low shock noise from power ON/OFF operation
- Better channel separation
- Fewer external components

■ Block Diagram



■ Absolute Maximum Ratings (Ta= 25˚C)

Parameter	Symbol	Rating	Unit
Supply Voltage Note 1)	V_{CC}	24	V
Supply Voltage Note 2)	V_{CC}	20	V
Supply Current	I_{CC}	4	A
Power Dissipation (Ta= 45˚C)	P_D	30	W
Operating Ambient Temperature	T_{opr}	– 30 ~ + 75	˚C
Storage Temperature	T_{stg}	– 55 ~ + 150	˚C

Note 1) Without signal V_{CC} = 24V (For non-stabilized supply)
Note 2) Operation V_{CC}= 20V (For stabilized supply)

■ Electrical Characteristics (Ta = 25˚C)

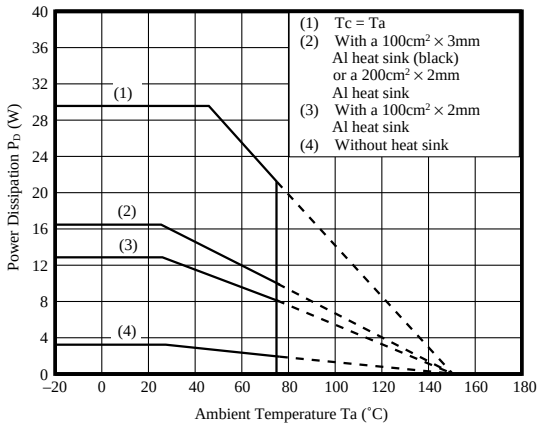
• V_{CC}=13.2V, R_L= 4Ω, f =1kHz

Parameter	Symbol	Condition	min.	typ.	max.	Unit
Quiescent Circuit Current	I_{CQ}	V_i = 0mV	40	70	120	mA
Voltage Gain	G_V	V_i = 3mV	52	54	56	dB
Output Power	P_O	THD = 10%	4.8	5.5	—	W
Total Harmonic Distortion	THD	V_i = 3mV	—	0.15	1	%
Output Noise Voltage	V_{no}	R_g = 10kΩ	—	1	3	mV
Channel Balance	CB	V_i = 3mV	—	0	1	dB
Separation	Sep.		45	50	—	dB
Ripple Rejection Ratio	RR	f = 60Hz, R_g = 600Ω	—	40	—	dB

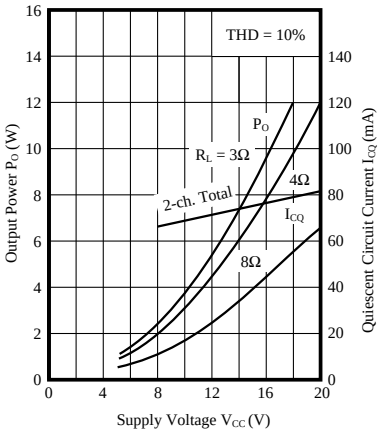
• V_{CC} =16V, R_L= 8Ω, f =1kHz

Parameter	Symbol	Condition	min.	typ.	max.	Unit
Quiescent Circuit Current	I_{CQ}	V_i = 0mV	40	80	140	mA
Voltage Gain	G_V	V_i = 4mV	52	54	56	dB
Output Power	P_O	THD = 10%	4	4.5	—	W
		R_L = 4Ω, THD = 10%	—	7.5	—	W
Total Harmonic Distortion	THD	V_i = 4mV	—	0.1	1	%
Output Noise Voltage	V_{no}	R_g = 10kΩ	—	1	3	mV
Crosstalk	CT	V_i = 4mV, R_g = 10kΩ	45	—	—	dB

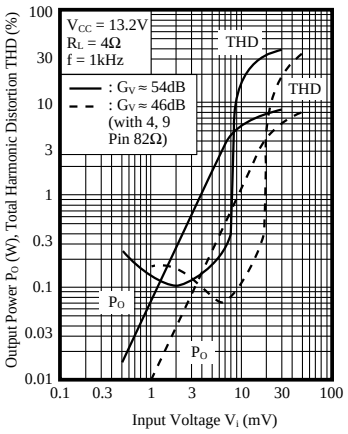
P_D – Ta



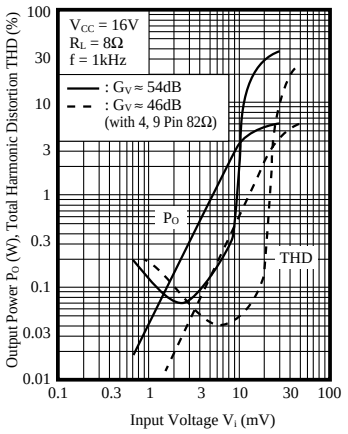
P_O, I_{CQ} – V_{CC}



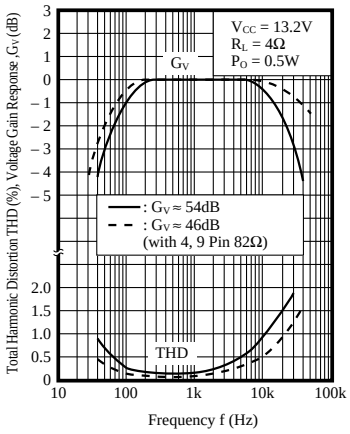
P_O, THD – V_i



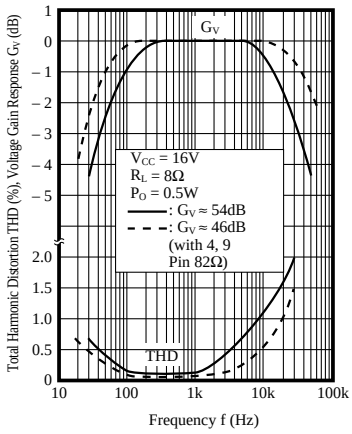
P_O, THD – V_i



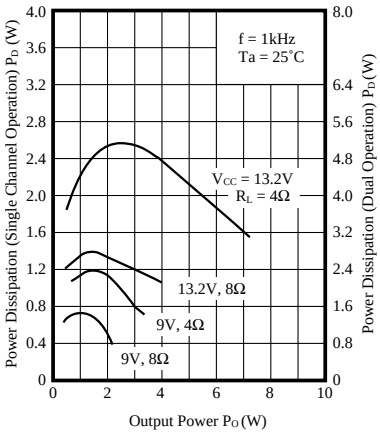
THD, G_V – f



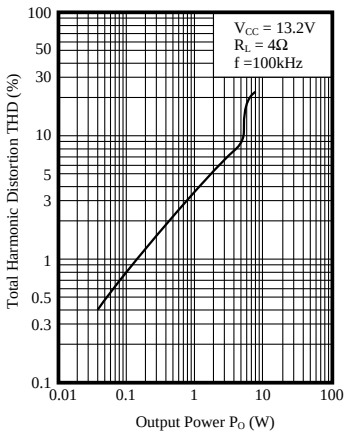
G_V, THD – f



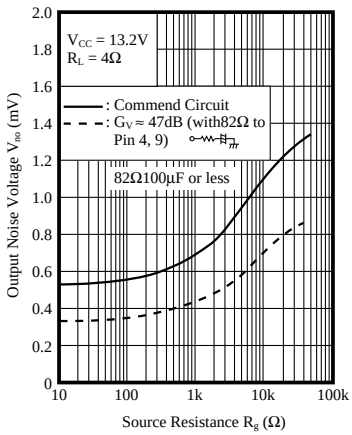
P_D – P_O

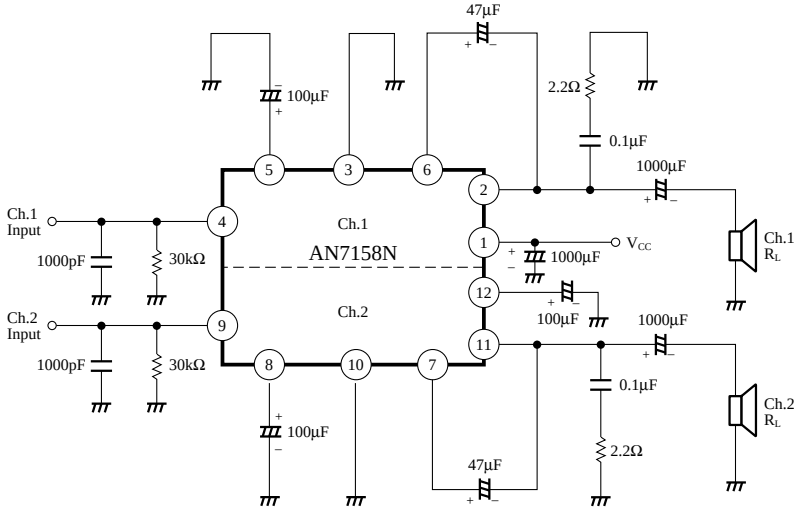


THD – P_O

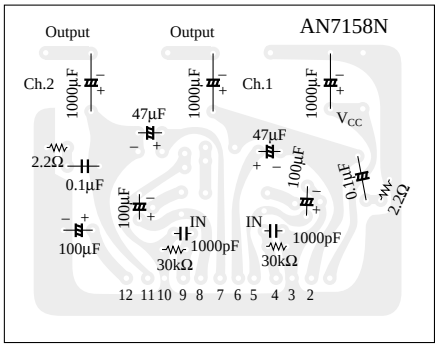


V_{no} – R_g





■ Printed Circuit Board Layout



■ Pin Descriptions

Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	7	Bootstrap Ch.2
2	Output Ch.1	8	N.F.B Ch.2
3	GND	9	Input Ch.2
4	Input Ch.1	10	GND
5	N.F.B Ch.1	11	Output Ch.2
6	Bootstrap Ch.1	12	Ripple Filter